CLAIMS

What is claimed is:

1. A zero-drift analog memory cell, comprising:

an input signal;

a sample signal having sample and hold states;

a tank for receiving the input signal and the sample signal and configured for generating and holding an output signal during the sample and hold states, respectively; and

a zero-drift transfer function (ZDF) feedback loop disposed in parallel with the tank and configured to maintain the output signal at a desired analog signal level during the hold state.

2. The zero-drift analog memory cell according to claim 1, wherein the ZDF comprises a diatonic function having a plurality of zero crossings.

3. The zero-drift analog memory cell according to claim 2, wherein the plurality of zero crossing comprises at least 5 zero-crossings.

4. The zero zero-drift analog memory cell according to claim 3, wherein the plurality of zero crossing further comprises at least 10 zero-crossings.

5. The zero-drift and hold analog dynamic memory cell according to claim 1, wherein the ZDF does not comprise an analog-to-digital (A/D) converter.

6. The zero-drift analog memory cell according to claim 1, wherein the ZDF feedback loop comprises:

a controlled oscillator (CO) for receiving the output signal and generating an oscillating signal; and

a harmonic frequency comparator (HFC) for receiving a reference signal and the oscillating signal and generating a correction signal input to the tank based on a

comparison between the frequency/phase of the oscillating signal and multiples of frequency on the reference signal.

7. The zero zero-drift analog memory cell according to claim 6, wherein the oscillating signal comprises a frequency monotonically correlated to the output signal.

8. The zero zero-drift analog memory cell according to claim 6, wherein the reference signal comprises a periodic signal having a reference frequency.

9. The zero-drift analog memory cell according to claim 8, wherein the reference signal further comprises a square wave having a duty cycle selected from the range greater than 0% up to about 50%.

10. The zero-drift analog memory cell according to claim 8, wherein the reference signal further comprises a signal having periodic pulses or spikes.

11. The zero-drift analog memory cell according to claim 8, wherein a frequency of the oscillating signal is greater than 5 times the reference frequency.

12. The zero-drift analog memory cell according to claim 8, wherein the reference frequency is greater than 5 times a frequency of the oscillating signal.

13. The zero-drift analog memory cell according to claim 8, wherein the reference frequency is stable during a hold state.

14. The zero-drift analog memory cell according to claim 6, wherein the CO comprises a voltage controlled oscillator.

15. The zero-drift analog memory memory cell according to claim 6, wherein the tank comprises an electronic circuit.

16. The zero-drift analog memory cell according to claim 6, wherein the tank comprises a capacitor.

17. The zero-drift analog memory cell according to claim 6, wherein the tank further comprises a high impedance buffer for receiving the output and outputting a buffered output.

18. The zero-drift analog memory cell according to claim 6, wherein the HFC comprises a nonlinear combination of the oscillating signal and the reference signal.

19. The zero-drift analog memory cell according to claim 18, wherein the nonlinear combination comprises multiplication.

20. The zero-drift analog memory cell according to claim 6, wherein the HFC comprises:

a multiplier for receiving the oscillating signal and reference signals and generating a modulated signal; and

a stability filter for receiving the modulated signal and generating the correction signal.

21. The zero-drift analog memory cell according to claim 20, wherein the stability filter comprises a transfer function to stabilized a feedback loop formed by the tank, CO and HFC.

22. The zero-drift analog memory cell according to claim 6, wherein the HFC comprises two transconductance amplifiers having outputs tied together for generating the correction signal.

23. The zero-drift analog memory cell according to claim 1, further comprising a switch for receiving the input signal and outputting the input signal in response to assertion of the sample state.

24. The zero-drift analog memory cell according to claim 23, wherein the tank comprises a transistor.

25. The zero-drift analog memory cell according to claim 6, wherein the input and output signals comprise analog voltages.

26. The zero-drift analog memory cell according to claim 6, wherein the input and output signals comprise optical signals.

27. The zero-drift analog memory cell according to claim 6, wherein the input and output signals comprise chemical signals.

28. The zero-drift analog memory cell according to claim 6, wherein the input and output signals comprise mechanical signals.

29. The zero-drift analog memory cell according to claim 6, wherein the input and output signals comprise magnetic signals.

31. A zero zero-drift analog memory array comprising a plurality of zero-drift and hold analog memory cells, each cell comprising:
an input signal;
a sample signal having sample and hold states;
a tank for receiving the input signal and the sample signal and configured for generating and holding an output signal during the sample and hold states, respectively; and
a zero-drift transfer function (ZDF) feedback loop disposed in parallel with the tank and configured to maintain the output signal at a desired analog signal level during the hold state.

32. The zero-drift analog memory array according to claim 11, wherein the ZDF feedback loop comprises:

a controlled oscillator (CO) for receiving the output voltage signal and generating an oscillating signal; and

a harmonic frequency comparator (HFC) for receiving a reference signal and the oscillating signal and generating a correction signal for input to the tank based on a comparison between the frequency/phase of the oscillating signal and multiples of frequency on the reference signal.

33. The zero-drift analog memory array according to claim 14, wherein the CO comprises a voltage controlled oscillator.

34. The zero-drift analog memory array according to claim 14, wherein the HFC comprises:

a multiplier for receiving the oscillating signal and reference signals and generating a modulated signal; and

a stability filter for receiving the modulated signal and generating the correction signal.

35. The zero-drift analog memory array according to claim 16, wherein the stability filter comprises a transfer function to stabilized a feedback loop formed by the tank, CO and HFC.

36. The zero-drift analog memory array according to claim 14, wherein the HFC comprises two transconductance amplifiers having outputs tied together for generating the correction signal.

37. A method for receiving an analog input signal and generating a stable analog output signal, said method comprising:

providing a tank for sampling and holding the input signal, during sample and hold states, respectively;

providing a zero-drift transfer function (ZDF) feedback loop in parallel with the tank circuit;

sampling the input signal during the sample state to generate an output signal; and

maintaining the output signal at a desired signal level by eliminating output signal drift using the ZDF feedback loop.

38. The method according to claim 37, wherein, providing the ZDF feedback loop comprises providing:

a controlled oscillator (CO) for receiving the analog output signal and generating an oscillating signal; and

a harmonic frequency comparator (HFC) for receiving a reference signal and the oscillating signal and generating a correction signal input to the tank based on a comparison between the frequency/phase of the oscillating signal and multiples of frequency on the reference signal.